REMARKS

Claims 8-10, 13-17 and 20-21 were examined. No claims are amended. Claims 8-10, 13-17 and 20-21 are pending.

The Patent Office rejects claims 8-10, 13-17, 20, and 21 under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 4,015,281 issued to Nagata et al. (Nagata) in view of U.S. Patent No. 5,990,516 issued to Momose et al. (Momose) and U.S. Patent No. 5,621,681 issued to Moon (Moon).

Regarding the rejection of claim 8, the Patent Office characterizes Nagata as showing the claimed relationship of a first material thickness and a second material thickness for a first and second dielectric material. The relationship in claim 8 is set forth as:

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox} \qquad (1)$$

According to the relationship, the sum of the thickness/dielectric constant of the first and second dielectric material equals a thickness/dielectric constant for a gate dielectric of silicon dioxide.

The Patent Office notes the relationship in Nagata shown at col. 4, lines 39-44:

$$T_{eff} = \left(\frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}} \right) E_{SiO_2}$$

To arrive at the relationship set forth in claim 8 (Equation (1)), the Patent Office rewrites Nagata to solve for T_{eff}/E_{SiO_2}.

Applicant has performed the operation noted by the Examiner. That operation set forth below.

$$\frac{T_{eff}}{E_{SiO_2}} = \frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}}$$

$$\frac{T_{eff}}{E_{SiO_2}} - \frac{T_{SiO_2}}{E_{SiO_2}} = \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}}$$

$$\frac{T_{eff} - T_{SiO_2}}{E_{SiO_2}} = \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}} \qquad (2)$$

In comparing equation (2) to equation (1), the equations are not identical. They can be similar if T_{eff}=0 and T_{SiO_2} is a negative number, which does not appear realistic in either case. Alternatively, solving for T_{SiO_2}/E_{SiO_2}, the Momose relationship may be represented as follows:

$$\frac{T_{SiO_2}}{E_{SiO_2}} = \frac{T_{eff}}{E_{SiO_2}} - \frac{T_{x1}}{E_{x1}} - \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet - \frac{T_{xi}}{E_{xi}} \bullet\bullet\bullet - \frac{T_{xn}}{E_{xn}} \qquad (3)$$

According to this relationship, equation (1) and equation (3) are not the same.

As noted in the response to Office Action filed October 26, 2004, neither Momose nor Moon describe a device having a gate dielectric relationship relative to a particular thickness for a gate dielectric of silicon dioxide.

For the above stated reasons, claim 8 is not obvious over Nagata in view of Momose and Moon. Claims 9-10 and 13-14 depend from claim 8 and therefore contain all the limitations of that claim. For at least the reasons stated above, claims 9-10 and 13-14 are not obvious over the cited references. In the final Office Action, the Patent Office notes that the claims do not specify a certain gate length. Applicant notes that claim 10 specifies a relationship between a gate length and a dielectric thickness, i.e., the combination of a first thickness and a second thickness of the dielectric materials is less than one-third of a length of the gate. The Patent Office also notes that the claims do not exclude SiO_2 as the second dielectric. Claim 13 specifies that the second dielectric material is selected from one of BST and PZT.

Regarding the rejection of claim 15, among other elements, claim 15 defines a semiconductor substrate having a transistor device formed thereon and having a gate dielectric

disposed between a surface of a substrate and a gate electrode. The gate dielectric includes a first dielectric material and a second dielectric material each having a material thickness determined by the relationship of equation (1) noted above. Thus, for the reasons noted above with respect to claim 8, claim 15 is not obvious over the cited references.

Claims 16-17 and 20-21 depend from claim 15 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 15, claims 16-17 and 20-21 are not obvious over the cited references. Applicant also notes the teachings of claim 17 relating dielectric thickness to gate length and claim 20 specifying a second dielectric material to address the concerns of the Patent Office that the claims do not specify a gate length or a second dielectric material.

Applicant respectfully requests that the Patent Office withdraw the rejection to claims 8-10, 13-17 and 20-21 under 35 U.S.C. §103(a).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 3/28/05

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon 3/28/05

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